REMARKS

Summary

Claims 1-9 were pending and all of the claims were said to be rejected in the subject Office action. Claim 10 has been introduced. No new matter has been added. The Applicants have carefully considered the Examiner's reasoning for the rejections, and respectfully traverse these actions based on the remarks to follow.

Rejection under 35 U.S.C. § 102 (e)

Claim 1 was rejected under 35 U.S.C. § 102 (e) as being anticipated by Belser et al. (US 5,737,344; "Belser"). The Applicants express their appreciation to the Examiner for the elaboration of the reasons for rejection given in the previous Office action. The Applicants also wish to amplify on their previous traverse, which is respectfully maintained.

> Claim 1 recites, *inter alia*, the processing circuit of said disk drive includes a low-level error-correction code unit for performing error correction of the data written to a physical address corresponding to a single sector of the disk, and the host computer includes a high level error correction code unit for performing error correction of the read data supplied through the interface and read from more than one sector of the disk.

Belser is directed towards a data storage method where a parity block is computed across a number of data sectors (Belser, 101), for example, on a bytewise basis, and separately stored in a parity sector. The teaching is an improvement on a transverse parity scheme to take account of a situation in which the individual data sectors are sparsely populated with data, and by doing so improves the ability of the parity data to reconstruct the data actually recorded in some special circumstances. As shown in Fig. 1, the prior art includes a sector ECC syndrome for each data sector, and this is a potential means of implementing step 704 in the data

processing sequence where a defective data item is detected. Belser teaches that the data processing sequence 702-716 can be performed by a processor of a data storage drive, a host computer or other digital processor (Belser, column 5, lines 63-66 and column 6, lines 20-26). Belser's teaches that the parity, computed by, for example an "exclusive or" (XOR) is used to correct an error detected in one sector of a data block (a defined group of multiple sectors). Since this is a parity method, it can only correct for single data errors. That is, if two or more of the sectors have errors, which cannot be corrected by the individual sector ECC syndrome, and those errors are in the same data element location in the respective sectors, the parity scheme cannot correct the error.

In contrast, the arrangement of Claim 1 "perform[s] error correction of the read data supplied through the interface and read from more than one sector of the disk." A parity scheme cannot do this.

As such, Belser does not teach or suggest the arrangement of Claim 1 where error correction of data read from more than one sector of the disk can be perfromed, and the claim is therefore not anticipated.

Rejection under 35 U.S.C. § 103(a)

Claims 1-9 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Hogan (US 6,252,961; "Hogan") in view of Demura et al. (US 6,357,030; "Demura"). The Applicants respectfully submit that the Examiner has not made out a *prima facie* case of obviousness on the basis of the references cited. Further, the obviousness rejections based on the Official notice assertions are respectfully traversed on the basis that the Examiner has merely adopted the teachings of the present application without presenting any independent evidence. In accordance with MPEP 707.05 at 700-88 and 37 CFR § 104 (d)(2), the Applicants respectfully reiterate the request that the Examiner provide an affidavit to support each of the rejections made on the basis of Official notice.

> Claim 1 recites, *inter alia*, the processing circuit of said disk drive includes a low-level error-correction code unit for performing error correction of the data written to a physical address corresponding to a single sector of the disk, and the host computer includes a high level error correction code unit for performing error correction of the read data supplied through the interface and read from more than one sector of the disk.

The arrangement of Claim 1 is distinguished from the references in that at least the low level error correction is performed in the disk controller and the high level error correction based on reading more than one sector of the disk is performed in the host computer.

Hogan is directed to a system of encrypting a data stream from a disk storage medium such that the error correcting code is preserved through the encryption process, and an entire block of data can be forwarded to the host computer across an insecure bus in a manner where the error correction process can be performed without decrypting the data. The data may then be again forwarded, while remaining encrypted, across an insecure bus architecture. In Hogan, the drive may have error correction capability, but if the error cannot be corrected then the entire block is sent to the host computer for error correction. (Hogan, column 4, line 66, bridging column 5, line 6). If the block was error free, or the block error correction worked at the drive level, then the block is forwarded directly to the user without being sent to the host. In both instances it appears that both the longitudinal and transverse error correction codes are employed at the drive level, and also, if required, at the host computer level. At least a full data block (e.g. 32kBytes) must be buffered in the drive. It is clear that Hogan refers to a block of data which is read from a multiplicity of sectors prior to being assembled into a logical data block for error correction and other processing. The entire block of data must be buffered since, as the occurrence of errors is random, an error is just as probably in the first byte of the block as in the

last byte of the block. Thus the operation is not performed on a sector-by-sector basis in the drive as in the arrangement of Claim 1. Hogan does not teach this aspect of the present arrangement and, thus, Hogan in conjunction with other references and Official notices does not teach all of the elements of the claim.

The Examiner asserts that Demura teaches "that it was well known in disk ECC for DVD to encode a higher level of ECC over multiple sectors of a lower level of ECC. Reading apparently progresses one sector at a time." (Office action page 3, third paragraph).

Demura is directed towards an efficient method of updating the block ECC values when less than the full contents of the data block are updated. This method is applied to the known art as described in Demura, and illustrated, for example, in Fig. 2 thereof. The data structure is said have data sectors, with a data block comprising 16 data sectors. The ECC is associated with the data block, while each sector has an "EDC (error detecting code)". (Demura, col. 1, lines 22-27). Demura specifically differentiates the function of the EDC applied at the sector level [low level] from ECC applied at the block level [high level]. If the two were the same, the same acronym would have been used. The Examiner's characterization of the reference as teaching that an ECC is applied at both high level and low level is thus not supported teachings of the reference. Only an EDC is applied at low level. The ECC is said to be capable of correcting a large number of errors (Id., col. 1, lines 37-38).

Only due to the Applicant's teachings has the Examiner been able to suggest a combination of the two references. There is nothing in the references themselves to suggest the desirability of the present arrangement, which minimizes the processing and memory requirements in the disk controller, processing the data one sector at a time, while allocating the higher level multi-sector error correction to the host computer.

Since the references cited do not teach all of the elements of the arrangement of Claim 1, nor is there any suggestion in the references to combine the teachings, there is no *prima facie* case of obviousness. Claims 2 and 3 are patentable, without more, as dependent claims further limiting an allowable claim.

No specific reason has been given for the rejection of independent Claim 4 in this Office action, and none was given in the previous Office action. Hence the Applicant respectfully submits that the allowability of this independent claim has been established. As Claims 5-9 are dependent on allowable Claim 4, they are likewise allowable.

Claims 2-9 are rejected under 35 U.S.C. §103(a) as being unpatentable over Belser in view of Sun (US 5,956,757; "Sun"). Claims 2-3 are claims dependent on Claim 1 and Claims 5-9 are dependent on Claim 4, both of which are allowable independent claims and are, without more, allowable.

New independent Claim 10 is presented. It is allowable for the same reason as Claim 4.

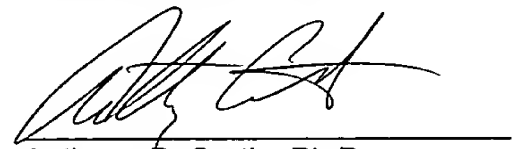
Conclusion

Claims 1-10 are pending.

For at least the reasons given above, the Applicants respectfully submit that pending Claims 1-10 are allowable.

The Examiner is respectfully requested to contact the undersigned in the event that a telephone interview would expedite consideration of the application.

Respectfully submitted,



Anthony P. Curtis, Ph.D.
Reg. No.:46,193
Agent for Applicants

BRINKS HOFER GILSON & LIONE
P.O. BOX 10395
CHICAGO, ILLINOIS 60610
(312) 321-4200